# Installing and Upgrading DDR3 Memory:
## Quick Reference Guide for NovaScale F2 Servers

### *Introduction*

This paper provides memory guidance at time of system purchase for later memory upgrades **NovaScale F2 Servers**. The purpose is to understand is supported, simplify terminology, and describe rules when installing memory with examples of upgrade paths.

### *Terminology Definitions*

DDR3 (Double Data Rate): The latest (3rd) generation of DDR DRAM; replaces DDR and DDR2 memory.

DIMM: Dual Inline Memory Module. This is the memory stick that is installed in each memory slot. It is comprised of multiple memory chips and, in some cases, registers, buffers and/or temperature sensors.

Dual Rank (DR): Two rows of DRAM comprising 64 bits of data each.

ECC (Error Checking and Correcting): This memory coding method is able to correct and identify certain types of DRAM and interface errors.

Enhanced ECC: Like ECC, but this memory coding method protects against additional memory error types including control line errors.

Hemisphere Mode: This mode allows interleaving between a processor's two memory controllers leading to improved performance. Interleaving also adds benefits to memory thermal performance by spreading memory accesses across multiple DIMMs and reducing memory "hot spots."

Lock-step: Pairs of DIMMs are accessed as a single double-wide (128-data bit) DIMM, allowing more powerful error-correction codes to be used, including detecting address errors.

MC: Memory Controller

Intel 7500 Scalable Memory Buffer: Translates one Scalable Memory Interconnect (SMI) bus into two DDR3 buses. Intel Xeon 7500 series processors must have this device to operate.

Mirror Mode (Mirroring): Two memory controllers are configured to allow the same data to be written to each. Each controller's data is identical to the other; thus, if one fails or has

multiple bit errors, there is a backup. The operating system will report half of your installed memory.

Quad Rank (QR): Four rows of DRAM comprising 64 bits of data each.

Rank: A row of DRAM devices comprising 64 bits of data per DIMM.

RAS: Reliability, Availability, and Serviceability

SDDC: Single Device Data Correction. Memory systems that utilize Single Device Data Correction can detect and correct multiple bit errors that come from a single memory chip on the DIMM.

Single Rank (SR): One row of DRAM comprising 64 bits of data.

Sparing (DIMM and Rank): The system allocates a Rank or DIMM per channel as a Spare memory region, and is able to move a Rank or DIMM exhibiting correctable errors to the Spare while the operating system is running.

RDIMM: Registered DIMMs. Address, Control, and Clock lines are buffered and re-driven on the DIMM.

## *Quick Reference Guide for NovaScale R440 F2, T840 F2 and R460 F2, T860 F2 servers:*

Table 1 is intended for quick reference in order to understand is supported and the rules governing memory configurations.

*Table 1: Quick Reference Memory Guide*

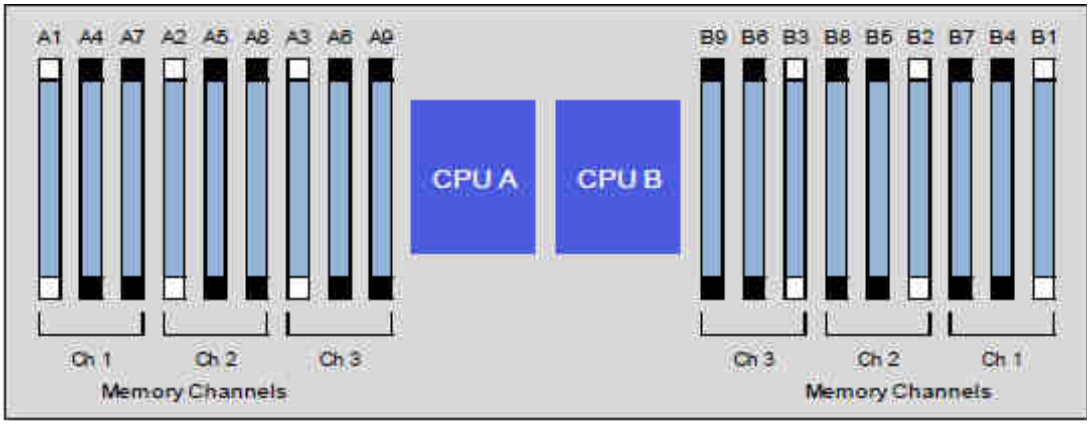
| DIMM Feature | Combine | Rules |
|---|---|---|
| Mixed Type (RDIMM / UDIMM) | No | Not Supported |
| Mixed Ranks | Yes | Single (SR) and Dual Rank (DR) DIMMs can be mixed. If mixing SR or DR with Quad Rank (QR) DIMMs, the first slot of each channel populated (first two white tab DIMM slots on each processor: A1, A2, B1 & B2) must be populated with the QR DIMM. Only two QR DIMMs are permitted per channel because the maximum of total ranks per channel is 8. |
| Mixed Capacity | Yes | All populated channels must have the same DIMM arrangement. Example with Channel 1: if bank A is populated with a 4GB DIMM (slot A1), bank B with 2GB (slot A4) and Bank C is empty (slot A7), all memory Channels must be populated that way. (see figure 5) |
| Mixed Speeds | Yes | If memory modules (DIMMS) with different speeds are installed, all DIMMs will operate at the speed of the slowest installed DIMM.<br>Also, if any DIMMS (regardless of speed) are installed in the third bank (bank C: slots A/B 7, 8 or 9), the maximum system memory speed will be 800MHz. This is the current maximum frequency supported by Intel and Dell, when DIMMS are installed in slots 7, 8 & 9. |
| Mixed Vendors | Yes | Any Dell sourced DDR3 DIMMs are supported, regardless of vendor or vendor mix. Where possible, Dell recommends using the same DIMM manufacturer. |

## *Identifying the correct DIMM slots in NovaScale R440 F2, T840 F2 and R460 F2, T860 F2 servers*

Pre-existing DIMM positions may not be correct for upgrading. When upgrading memory modules, you must follow these population guidelines. ***Incorrect population will result in BIOS warnings or errors.***

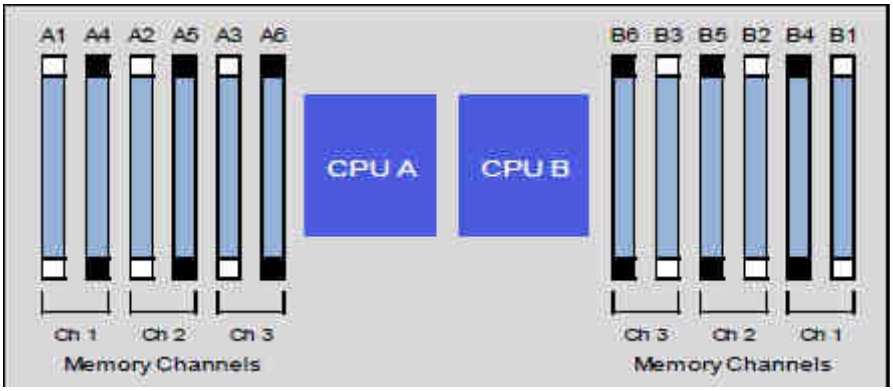
***R460 F2 / T860 F2***

***Figure 1: This is the physical memory layout on the servers (technical schematic). White tabs indicate first slot of each channel.***




***R440 F2 / T840 F2***

***Figure 2: This is the physical memory layout on the servers (technical schematic). White tabs indicate first slot of each channel.***

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## *Overview Intel Architecture*

NovaScale R460 F2 & T860 F2 servers use the new Intel® Xeon™ 5500/5600 series CPUs that support the new DDR3 memory technology. Each CPU has three separate memory controller hubs (MCHs). Figure 1 illustrates this new CPU architecture and memory layout for 18 DIMM systems – the R460 F2 and T860 F2 servers.

Due to this new technology, there are limitations on memory speed. Total system memory speed is dependent on the CPU, DIMMs populated per channel, and the DIMM ranking. For example, one restriction is that Quad Rank (QR) DIMMs must be the first DIMM installed in a channel (memory bank #1)*

***Note that only two Quad Rank DIMMs may be installed per channel. This is due to the **limitation of only having 8 total ranks per channel.**

- Single Rank (SR): one row of DRAM comprising 64-bits of data.
- Dual Rank (DR): two rows of DRAM comprising 64-bits of data each.
- Quad Rank (QR): four rows of DRAM comprising 64-bits of data each.

***Figure 3: R460 F2, T860 F2 Servers memory illustration (not a technical schematic of motherboard)***

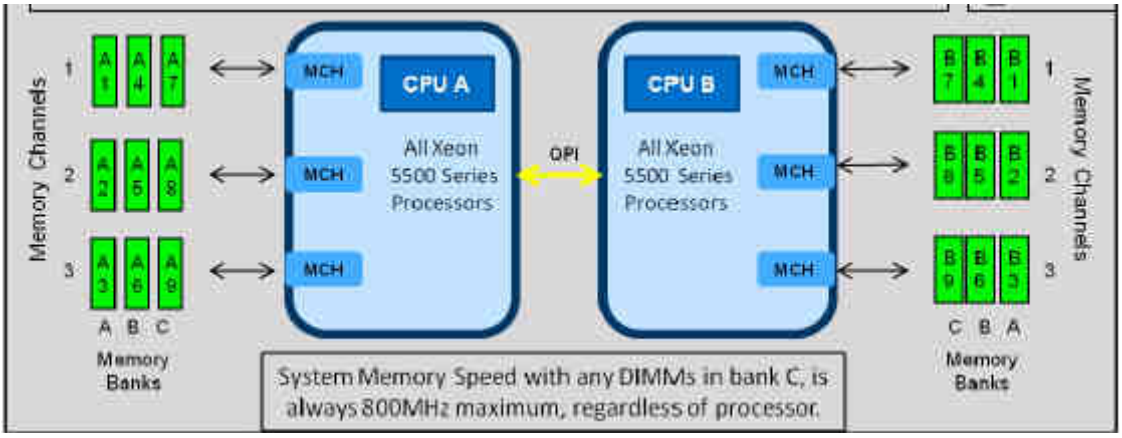
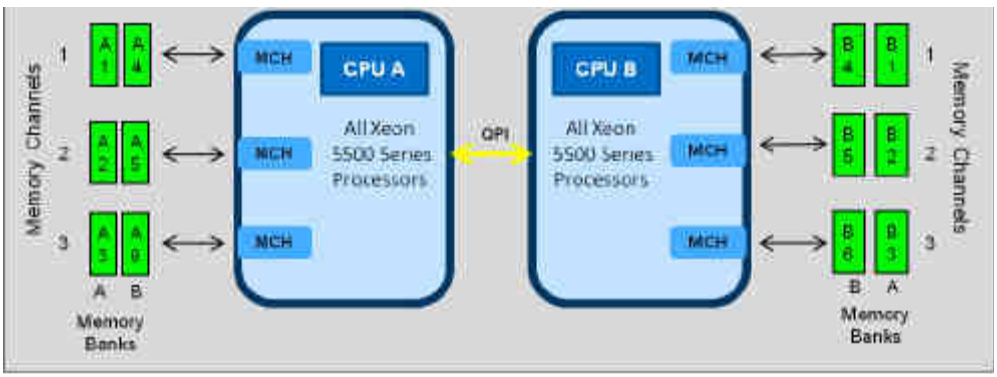



**Figure 4 R440 F2, T840 F2 Servers memory illustration (not a technical schematic of motherboard)**

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## *Balanced Memory Configuration*

Any DIMM configuration that **does not adhere** to the guidance below is "**unbalanced"** and generally not recommended. Unbalanced configurations can potentially generate BIOS warnings or error messages. The only exceptions to this statement are a few low DIMM count offerings and specific configurations for RAS features (such as Advanced ECC and Mirroring) which only populate 2 channels and do not use the third channel.

A **Balanced Memory Configuration** is a memory configuration where both CPU 1 and CPU2 (if installed) both have identical memory populations on all memory channels. This does not mean all the DIMMs must be the same size/capacity. "Balanced" means that the same size/capacity DIMM must be installed in the **same memory bank** on every populated memory **channel. Bank A must have all the same DIMMS installed in every populated slot. Bank B must have all the same DIMMS installed in every populated slot. Bank C must be done in the same way fashion.**

Figure 5 provides an example of a balanced configuration on the R460 F2, T860 F2

***Figure 5: This is an example of a balanced memory configuration for the R460 F2, T860 F2 with 36GBs of memory (6 x 4GB and 6 x 2GB). (Not a technical schematic of motherboard***

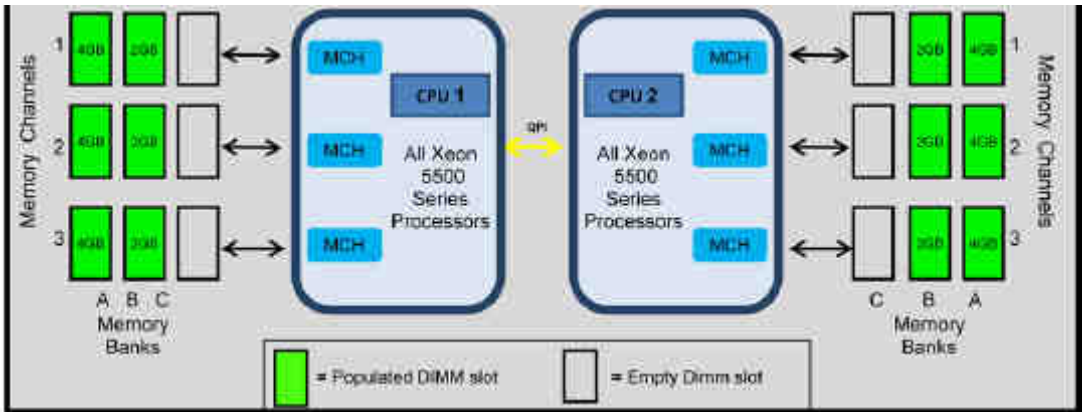
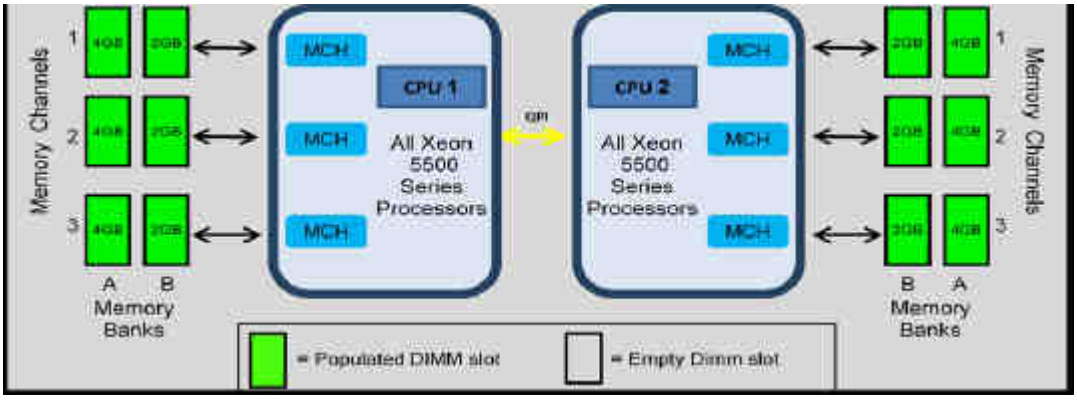



Figure 6 provides an example of a balanced configuration on the R440 F2, T840 F2

***Figure 6: This is an example of a balanced memory configuration for the R440 F2, T840 F2 with 24GBs (6 x 4GB) of memory. (Not a technical schematic of motherboard)***



## *NovaScale 1Gb to 2Gb Memory Transition: Impact on RAS Features*

Aligning with the industry shift of DDR3 memory technology, 1Gbit DRAM-based DIMMs move to **2Gbit DRAM-based DIMMs**. This 2Gbit technology offers DIMMs with reduced ranks and lower power consumption and enables the replacement of 4GB (gigabyte) 1066 QR DIMMs with 4GB DR 1333 DIMMs.
With this memory transition, three DIMMs (see chart below) move from x4 to x8 DRAM in NovaScale F2 servers, thereby eliminating Single Device Data Correction (SDDC) capability in Optimized mode on x8 DRAM. Even though SDDC is not available with x8 DIMMs, it should be noted that the error correcting schemes allowing x4 SDDC are still in play.

**Two options in this transition.**
**1.** Opting for Advanced ECC which offers SDDC for both x4 and x8 based DIMMs.
**2.** Or, x4 DIMMs (8GB 2Rx4) can still be purchased which allows for SDDC in Optimized mode.

**Impacted DIMMs:**

| Current DIMM Description | Replacement DIMM Description |
|---|---|
| DIMM,4G,1333,2RX4X72, | DIMM,4G,1333,2RX8X72, |
| RDIMM, 4GB, 1333, 2RX4, 1Gb, LV | RDIMM, 4GB, 1333, 2RX8, 2Gb, LV |
| RDIMM, 4GB, 1333, 2RX4, 1Gb | RDIMM, 4GB, 1333, 2RX8, 2Gb |

## *Quick Reference Guide for NovaScale R480 F2 servers:*

### Overview Intel Architecture

NovaScale R480 F2 4-socket servers use the new Intel Xeon 7500 series processors that support DDR3 memory technology. Each processor has two memory controllers that support two Millbrook Memory Buffers. Every Millbrook Memory Buffer supports up to four DIMMs, which allows for greater scalability and memory performance.

It is important to recognize that memory speed and the processor chosen have interdependencies. The processor's maximum QuickPath Interconnect (QPI) speed will determine the memory performance (1066 MTS, 978 MTS, or 800 MTs). Memory speed remains locked regardless of DIMM population. There is no speed change when populating increasing numbers of DIMMs. However, there are recommended population practices when upgrading or changing memory. DIMMs always must be populated identically in pairs (A1-A2, for example).

**Table 1.** Quick Reference R480 F2 Memory Guide

| DIMM Feature | Combine | Rules |
|---|---|---|
| Mixed Ranks | Yes | DIMMs of different Ranks can be mixed. The first slot of each channel populated (first two white tab DIMM slots on each memory buffer: A1, A2, A3, and A4) must be populated with the highest ranked DIMM. |
| Mixed Capacity | Yes | DIMMs must match (capacity, rank) across channels. For example, a 1 GB RDIMM in A1 and A2 implies that A3 and A4 would need to be 1 GB RDIMMs also. DIMM slots A5, A6, A7, and A8 could be a different capacity and rank. |
| Mixed Speeds | Yes | Nehalem EX Architecture will support a maximum memory speed of 1066 MTs. |
| Mixed Vendors | Yes | Any Dell-sourced DDR3 DIMMs are supported, regardless of vendor or vendor mix. Where possible, Dell recommends using the same DIMM manufacturer. |

**Note:** Only RDIMMS are supported with Intel 7500 processors

**Table 2.** Quick Comparison Intel Xeon 5500-5600 Series to Intel Xeon 7500-6500

| Feature | Intel Xeon 5500-5600 Series | Intel Xeon 7500-6500 Series |
|---|---|---|
| DIMM Type | DDR3 (UDIMM or RDIMM) | DDR3 (RDIMM only) |
| DIMM Rank | DR, SR, or QR | DR, SR, or QR |
| All Memory channels operate at the same frequency | Yes | Yes |
| Memory controllers per socket | 1 | 2 |
| Memory Channels per socket | 3 | 4/8<br>(4 SMI Buses/8 DDR3 Channels) |
| Maximum DIMMs per channel | 3 | 2 |
| DIMM Speed<br>(Speed shown is for top bin...may be slower for down- | 1333 MTs (1 and 2 DPC)<br>1066 MTs (2 DPC)<br>800 MTs (3 DPC) | 1066 MTs (1 or 2 DPC)<br>(Same speed for SR, DR, or QR DIMMs) |
| bin SKUs) | (Slower with QR DIMMs) | |
| Minimum memory population | 1 DIMM | 2 DIMMs<br>(must populate with identical DIMM pairs) |
| Hemisphere Mode | No | Yes |
| Memory RAS Features | ECC, DIMM Sparing, Lock-step, Mirroring, x4 or x8 SDDC | Enhanced ECC, DIMM sparing, Lock-step, Mirroring, x4 or x8 SDDC, Rank sparing |

**NovaScale R480 F2 servers**

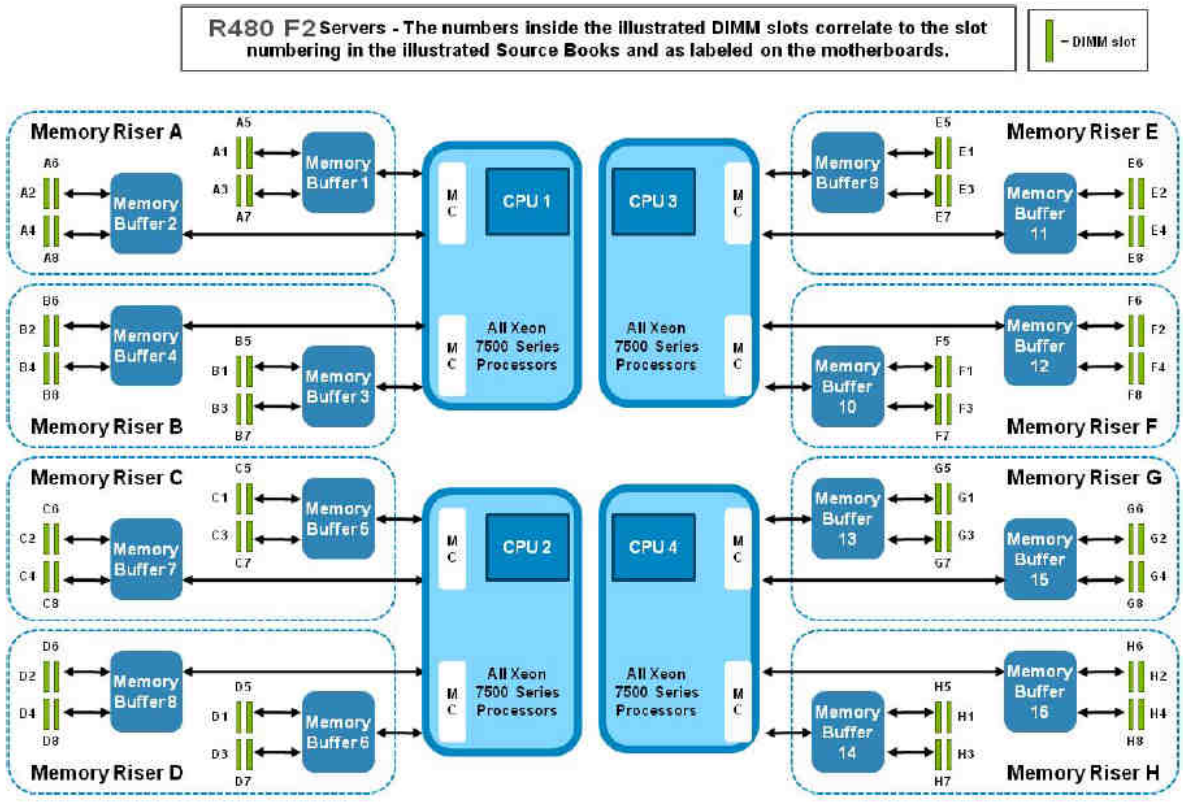
The R480 F2 utilizes DDR3 memory providing a high performance, high-speed memory interface capable of low latency response and high throughput. The R480 F2 supports RDIMMs only.

The R480 F2 utilizes Intel Xeon 7500 series processors that have one memory controller hub and two integrated memory controllers. Each of those memory controllers has two SMI channels that connect to the Intel 7500 Scalable Memory Buffer.

The DDR3 memory interface consists of 16 Intel 7500 Scalable Memory Buffers, each of which has two DDR3 memory channels. Each channel supports up to two RDIMMs (single/dual/quad-rank). By limiting to two DIMMs per DDR channel, the system can support DIMMs running at 1066 MTs.

The R480 F2 has eight memory risers; each memory riser has two Millbrook memory buffers and eight DIMM slots.

Figure 3. R480 F2 Servers Memory Illustration




**Note:** This illustration is not a technical schematic of a motherboard. DIMMs in Risers A and B correspond to CPU 1, DIMMs in Risers C and D correspond to CPU 2, DIMMs in Risers E and F correspond to CPU 3, and DIMMs in Risers G and H correspond to CPU 4. A CPU must be present to populate the riser. A system can operate with only one riser per CPU.

## Optimizing Memory Performance for Intel Xeon 7500 and 6500 Series Processors

Intel Xeon 7500 Series processors support a maximum memory performance of 1066 MTs.

***Best Performance***
2 DIMMS per Memory Buffer Channel, all memory controllers populated equally with 64 DIMMs and 8 Memory Risers (see Figure 4), highest bandwidth and lowest latency

***Better Performance***
1 DIMM per Memory Buffer Channel, all memory controllers populated equally with 32 DIMMs and 8 Memory Risers (see Figure 5), slight bandwidth decrease

***Good Performance***
2 DIMMS per Memory Buffer Channel, all memory controllers populated equally with 32 DIMMs and 4 Memory Risers, lower maximum bandwidth, higher latency
1 DIMM per Memory Buffer Channel, all memory controllers populated equally with 16 DIMMs and 4 Memory Risers, lower maximum bandwidth, higher latency

**Note:** Mixed DIMM capacity is supported. The recommendation is to populate memory controllers equally and always pair DIMMs identically.

**Figure 4. R480 F2 Relative Memory Bandwidth for the Intel Xeon 7500 Series Processors**

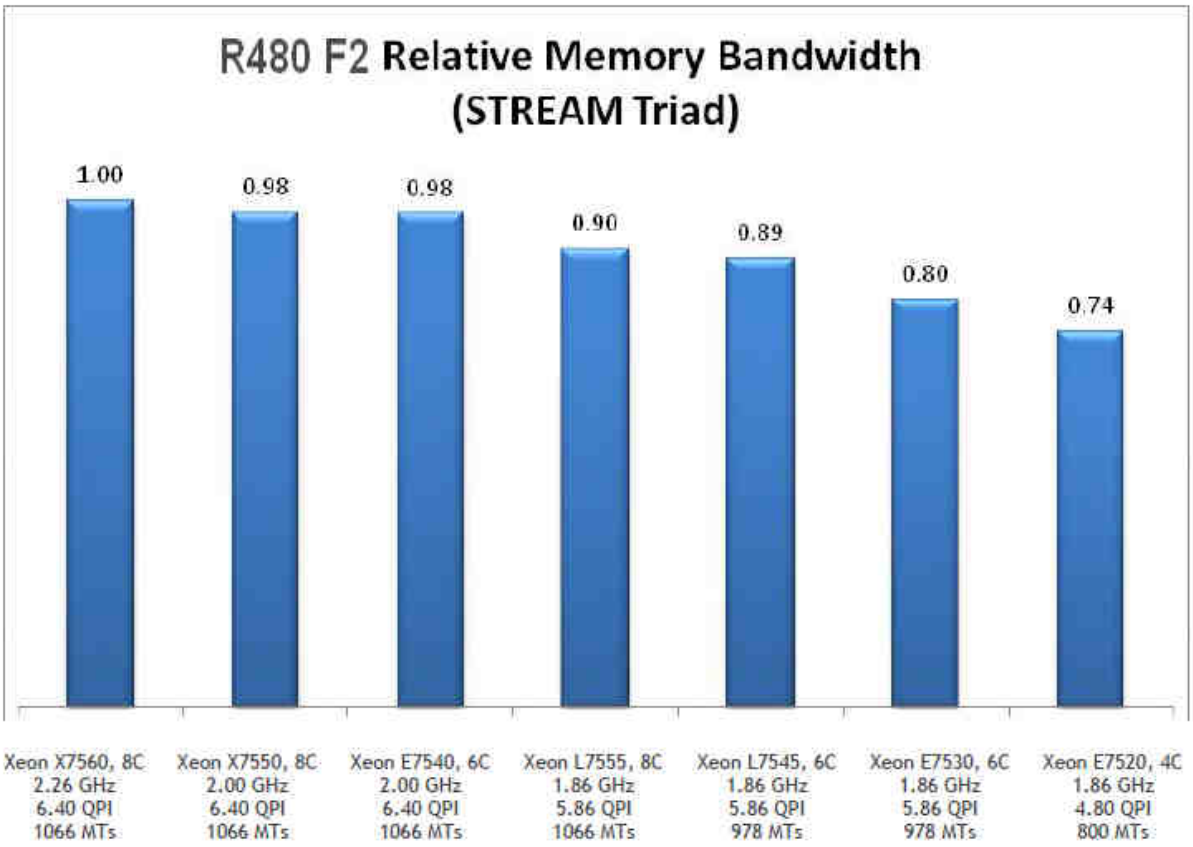


**Figure 5. R480 F2 With64 Identical DIMMs,2 DIMMs Per Channel**

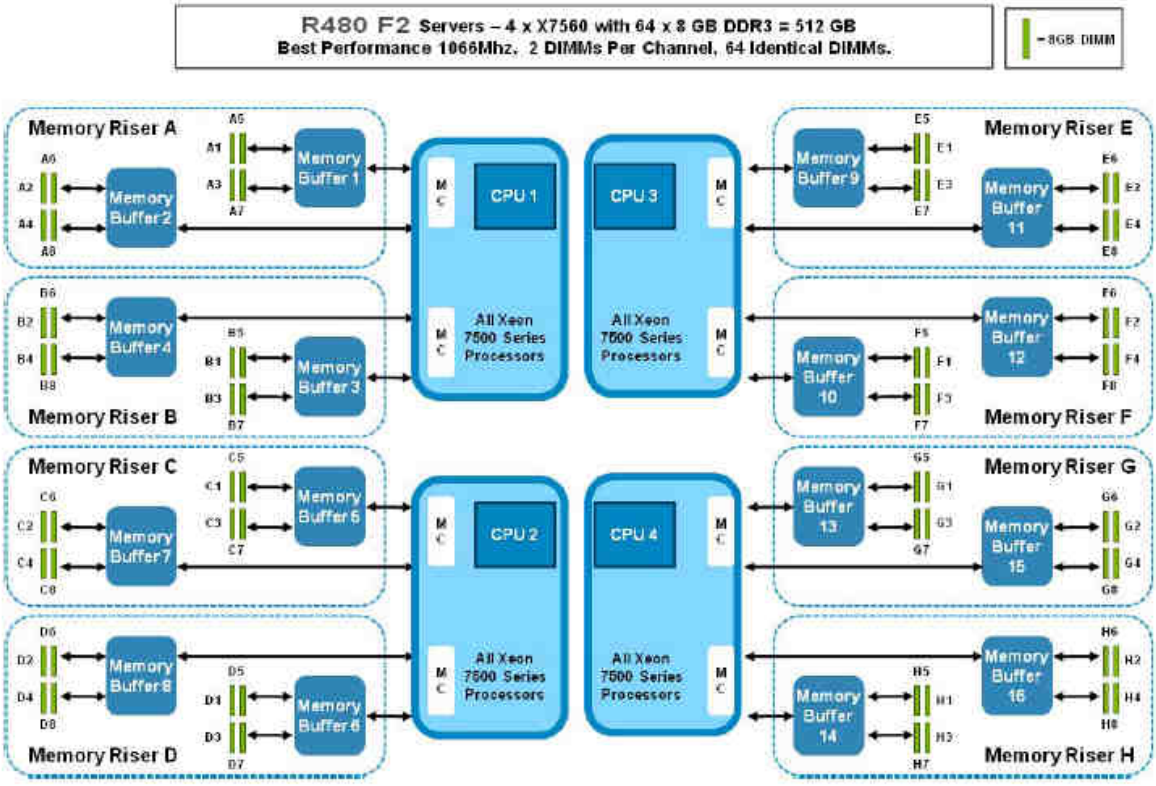
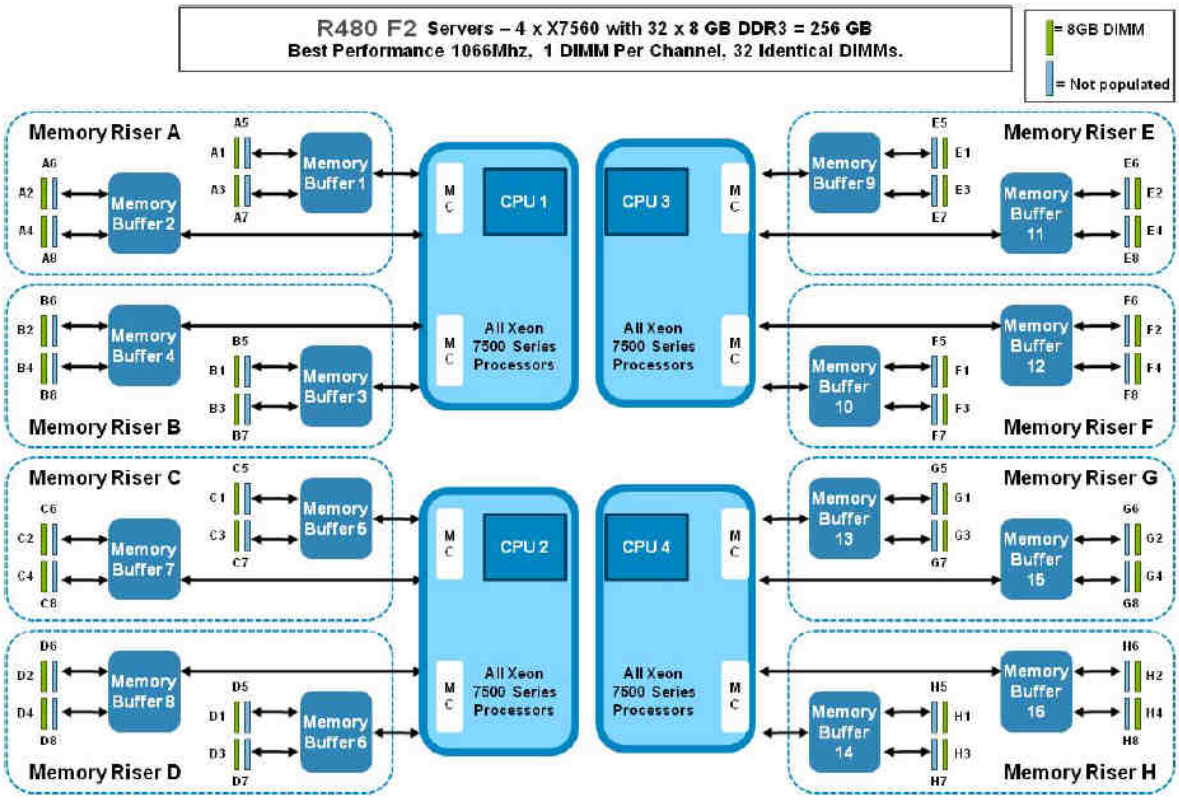



**Figure 6. R480 F2 With 32 Identical DIMMs, 1 DIMM Per Channel**



## Memory RAS Features

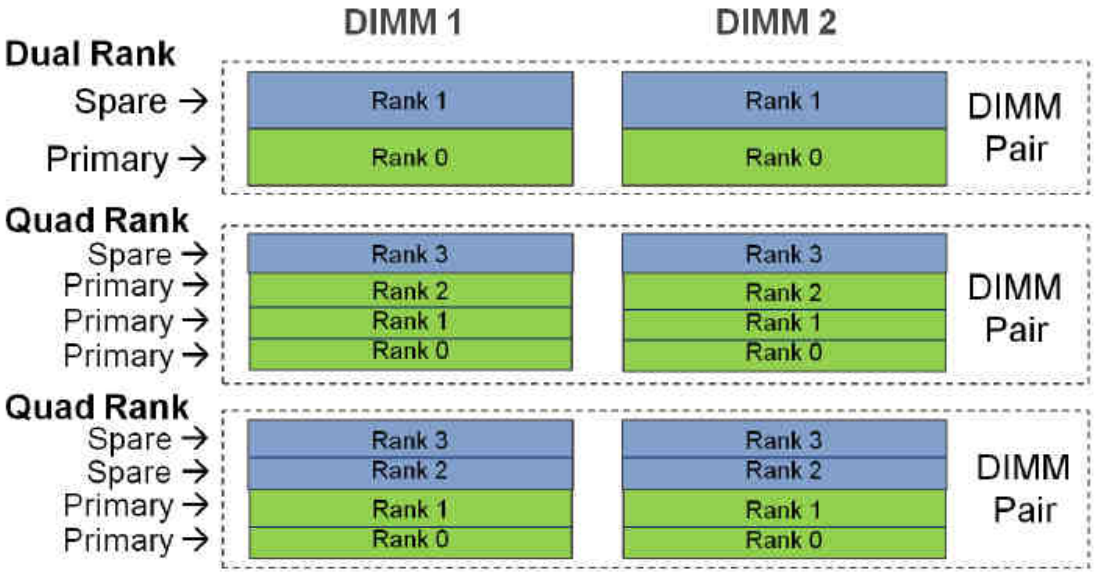
### *Sparing*

For Rank sparing, one rank on each lock-step Millbrook pair will be reserved as a spare, and in the event that another rank exceeds a threshold of correctable ECC errors, the "failing" rank will be copied to the spare. After that operation is complete, the failed rank will be disabled.

For Dual rank DIMMs: 1 rank within a DIMM is used as a spare

For Quad rank DIMMs: 1 or 2 ranks within a DIMM are used as a spare

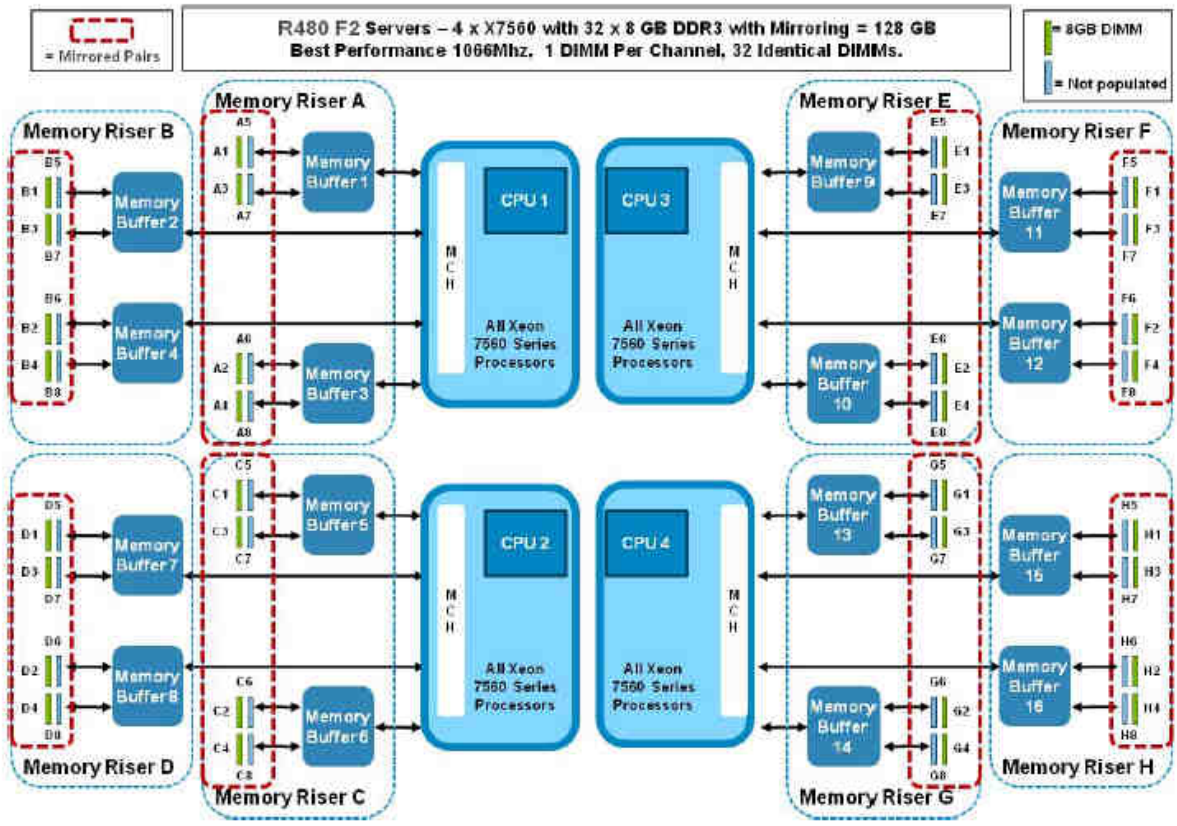
**Figure 7. Example of Sparing for Dual Rank and Quad Rank DIMMs**




### *Mirroring*

For mirroring, the R480 F2 will support 2P/4P configurations for >= 64 GB only. When mirroring is enabled, only half of the physical memory will be visible to the system. A full copy of the memory is maintained, and, in the event of an uncorrectable error, the system will switch over to the mirrored copy. The R480 F2 uses intra-socket mirroring.

**Figure 8: Example of R480 F2 Intra-Socket Mirroring**




Note: A1, A3 are mirrored to A2, A4; B1, B3 are mirrored to B2, B4; C1, C3 are mirrored to C2, C4; D1, D3 are mirrored to D2, D4; E1, E3 are mirrored to E2, E4; F1, F3 are mirrored to F2, F4; G1, G3 are mirrored to G2, G4; H1, H3 are mirrored to H2, H4.

**Table 3. Intel Xeon 7500/6500 Series Processor Performance and Max Memory Speed**

| Intel Xeon Processor | Max Memory Speed |
|---|---|
| 130 Watt X7560* | 1066 MTs |
| 130 Watt X7550* | 1066 MTs |
| 130 Watt X7542* | 978 MTs |
| 105 Watt E7540 | 1066 MTs |
| 105 Watt E7530** | 978 MTs |
| 95 Watt E7520 | 800 MTs |
| 95 Watt L7555 | 978 MTs |
| 95 Watt L7545 | 978 MTs |